REMARKS

In the Drawings

Applicant notes the Examiner has objected to the drawings filed July 28, 2000. Applicant submitted a Red-lined Figure 1A and Thirty-eight (38) sheets of formal drawings March 11, 2004. Figure 1A was amended to correct a typographical error. Applicant also submitted supporting amendments to the specification.

Applicant has submitted courtesy copies of Red-lined Figure 1A and Thirty-eight (38) sheets of formal drawings for the Examiner's review.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-15 and 28-38 were rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Akaogi et al. (U.S. Patent No. 6,240,040). Applicant respectfully traverses this rejection. Applicant reserves the right to swear behind the reference Akaogi et al., but submits that claims 1-15 and 28-38 are allowable for the following reasons.

Each of claims 1, 6 and 33, recites an array of non-volatile memory cells arranged in a plurality of addressable banks and a plurality of bank buffers, the bank buffers and addressable banks coupled one to one, where each of the plurality of bank buffers is adapted to store data from a row of memory cells contained in its corresponding addressable bank of the plurality of addressable banks.

Applicant carefully reviewed Akaogi et al. and found no indication of a plurality of bank buffers and a plurality of addressable banks that are coupled one to one, as in each of claims 1, 6 and 33. Instead, Figure 2 of Akaogi et al. shows a single sense amplifier block 268, and not a plurality of buffers. The single sense amplifier block 268 may include an output buffer or a data latch to assist its operation and can be selectively coupled to a single bank of plurality of memory banks (202, 204, 206, 208) at a time. *See, e.g.*, Akaogi et al. Figure 2, column 7, lines 43-63, and column 9, lines 8-45. Therefore, Akaogi et al. does not include each and every element of each of claims 1, 6 and 33, and claims 1, 6 and 33 should be allowed over Akaogi et al.

Claims 2-5 and 28 depend directly or indirectly from claim 1 and thus include patentable limitations of claim 1. Claims 7-10 and 29-31 depend directly or indirectly from claim 6 and thus include patentable limitations of claim 6. Claims 34-38 depend directly or indirectly from claim 33 and thus include patentable limitations of claim 33. Therefore, claims 2-5, 7-10, 28-32, and 34-38 should be allowed.

Claim 11, recites copying first data stored in a row of a first non-volatile memory cell array bank to a first buffer circuit using control circuitry of the memory, copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit using the control circuitry, performing a write operation to write third data to the first array bank using a first external processor coupled to the flash memory, reading the first data from the first buffer circuit using the first processor while performing the write operation, and reading the second data from the second array bank using a second external processor coupled to the flash memory while performing the write operation.

As stated above, Akaogi et al. does not teach or disclose copying first data from a first array bank to a first buffer and then reading the first data from the first buffer while simultaneously writing a third data to the first array bank. Akaogi et al. therefore does not include copying second data stored in a row of a second non-volatile memory cell array bank to a second buffer circuit and reading the second data from the second array bank using a second external processor coupled to the flash memory while performing a write operation to write third data to a first array bank using a first external processor. Therefore, Akaogi et al. does not include each and every element of claim 11, and claim 11 should be allowed.

Claims 12-15 and 32 depend directly or indirectly from claim 11 and thus include patentable limitations of claim 11. Therefore, claims 12-15 and 32 should be allowed.

Applicant respectfully contends that claims 1-15 and 28-38 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1-15 and 28-38.

Double Patenting Rejection

The Examiner provisionally rejected claims 1-27 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of co-pending U. S. Patent Application Serial No. 09/628,184 (the '184 application). Applicant respectfully traverses this rejection.

The Examiner had previously rejected claims 1-27 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of the co-pending '184 application in the Office Action mailed October 6, 2003. In the present Office Action mailed May 17, 2004, the Examiner further stated in regards to the double patenting rejection that "[a]though the conflicting claims are not identical, the are not patentably distinct from each other because every feature of the claims of the present invention which was either explicitly taught or would have been obvious in view of the limitations of claims 1-23 of the copending application. The only difference between the present claims and the claims of the '184 application is that the present claims utilize a read buffer (output buffer) for the Flash banks. Both sets of claims recite simultaneous reading and writing to flash memory banks, however the present claims include the obvious and well known use of a read buffer during such operation."

The Applicant maintains, as in the Response mailed December 19, 2003, that claims 1-27 of the present application include simultaneous writing to an array bank while reading data from a dedicated read buffer connected to same array bank, where the data has been copied from the array bank to the buffer. The claims 1-27 of the present application also require that these bank read buffers are coupled one to one to their associated banks. A separate output buffer is utilized by the memory of the present invention to facilitate output of the data from the memory device from any of the memory bank read buffers. In contrast, the '184 application does not teach individual bank read buffers and thus cannot simultaneously read and write to the same bank. The claims 1-23 of the '184 application include writing data to one bank of a plurality of addressable banks of an array of non-volatile memory cells and simultaneously reading data from another bank of the plurality of addressable banks of the array of non-volatile memory cells.

In addition, the Applicant further contends that there is no motivation or suggestion to modify the '184 application in this manner. Specifically, Applicant contends that to modify the '184 application to provide writing to a single bank of a memory array while reading from the same bank of the memory array would require a modification of the '184 application's memory array to include read buffers coupled one to one with the array banks and to allow the reading of buffered read data from a bank of a memory array while writing to the same bank. Applicant finds no motivation or suggestion to modify the operation of '184 application expressly or impliedly contained in the '184 application reference as the memory disclosed by the '184 application already includes an output buffer, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention of claims 1-27 to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Therefore, claims 1-27 of the present application are patentably distinct from claims 1-23 of the '184 application because claims 1-27 of the present application require non-obvious limitations not included in claims 1-23 of the '184 application. The rejection of claims 1-27 under the judicially created doctrine of obviousness-type double patenting should be removed, and claims 1-27 allowed.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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